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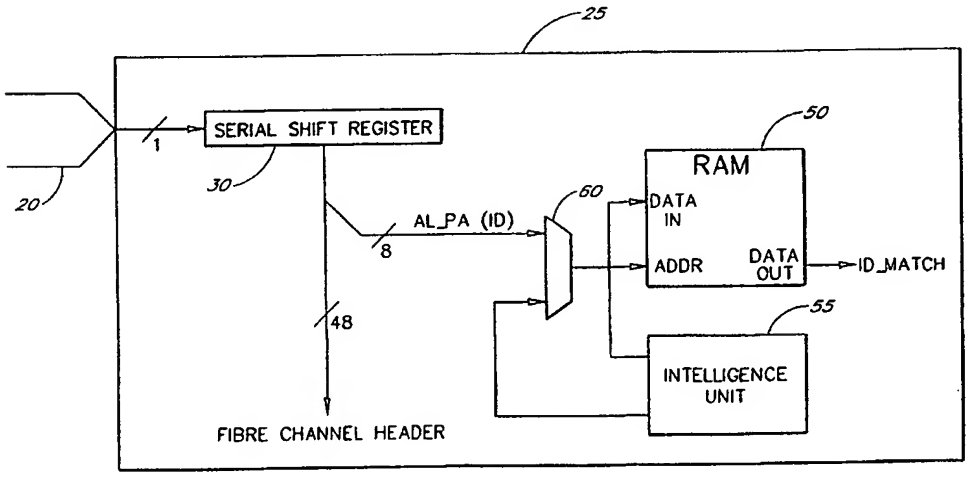
(54) Title: METHOD AND APPARATUS FOR COMPARING AN ADDRESS SENT ON A BUS TO A DEVICE'S ASSIGNED ADDRESS OR ADDRESSES



(57) Abstract

A method and an apparatus compare addresses sent on an interconnect system with a device's own assigned address or addresses. The interconnect system may be a Small Computer Standard Interface (SCSI) bus, a Fiber Channel, or any other environment which uses numeric addresses to identify devices. The method and apparatus allow a device to respond to multiple addresses received from a bus without the use of registers and logic circuits for each address. The apparatus comprises a random access memory (RAM) with a plurality of memory locations. The memory locations correspond to possible addresses which may be assigned to the device. The RAM stores a '1' in each memory location corresponding to one of the device's assigned addresses, and stores a '0' in each memory location not corresponding to one of the device's assigned addresses. The RAM further comprises an address input which receives an address from the bus. The RAM also comprises a data output which informs the device whether the address received from the bus matches one of the device's assigned addresses.

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METHOD AND APPARATUS FOR COMPARING AN ADDRESS SENT ON A BUS TO A DEVICE'S ASSIGNED ADDRESS OR ADDRESSES

Background of the Invention

Field of the Invention

The present invention relates to data communication. Specifically, the present invention relates to a method and apparatus which compares addresses sent on a bus with a device's own assigned address or addresses.

Brief Description of the Related Art

Currently, a device connected to a bus must compare a numeric address or ID on the bus to the device's own assigned numeric ID to determine if the impending transaction is intended for that particular device. This is normally achieved by a hardware register which contains a device's assigned numeric ID value and a comparison logic circuit to compare the contents of the register with the ID value on the bus. If the comparison logic circuit indicates that the two ID values are the same, then the device assumes that it is included in the impending transaction transmitted on the bus.

Summary of the Invention

The present invention relates to a method and apparatus which compares addresses sent on a bus (interconnect system) with a device's own assigned address or addresses. For example, the device may be an I/O subsystem, a disk drive, a printer, a modem or a fax machine. The present invention is ideally suited for devices that can make use of multiple addresses, such as an I/O subsystem.

Conventionally, existing devices use hardware registers and comparison logic circuits to determine if the impending transaction is intended for a particular device. If a device needs to respond to more than one ID, a separate hardware register and a separate comparison logic circuit must be provided for each ID that the device is required to respond to when the ID is sent on the bus. This can result in a significant amount of hardware. The bus or interconnect system may be a Small Computer Standard Interface (SCSI) bus, a Fiber Channel, or any other environment that identifies a device using a numeric ID. For a SCSI bus, a device requires sixteen registers and sixteen comparators to enable the device to respond to all addresses on the bus. In a Fiber Channel, the number of separate circuits may be as high as 125. Due to its high speed and its serial nature, a Fiber Channel presents a particular difficulty in supporting multiple IDs.

The present invention provides a method and apparatus which allows a device to respond to any number of device IDs on a bus with a significant reduction in hardware real estate and costs, and no impact on the speed of recognizing a matching ID.

In one embodiment, the apparatus comprises a random access memory (RAM) with a plurality of memory locations. The memory locations correspond to possible addresses which may be assigned to the device. The RAM stores a '1' in each memory location corresponding to one of the device's assigned addresses, and a '0' in each memory location not corresponding to one of the device's assigned addresses. The RAM further comprises an address input which receives an address from the bus. The RAM also comprises a data output which informs the device whether the address received from the bus matches one of the device's assigned addresses.

Brief Description of the Drawings

Figure 1 illustrates a processor, an interconnect system and at least one device in communication with the interconnect system.

Figure 2 illustrates registers and compare logic circuits related to a device in Figure 1.

Figure 3 illustrates one embodiment of the present invention.

Detailed Description of the Preferred Embodiments

The present invention is suited for any environment that uses numeric IDs to identify particular devices connected to the bus (interconnect system). The description below focuses on one of these environments, the Fiber Channel, but those of ordinary skill in the art will appreciate that the present invention may be used with other interconnect systems, such as a SCSI bus. The present invention is ideally suited for devices that can make use of multiple addresses, such as an I/O subsystem.

Figure 1 illustrates a system 10 which comprises a host or processor 15, an interconnect system 20 and at least one device 25 in communication with the interconnect system 20. In one embodiment, the interconnect system 20 is a bus. In another embodiment, the interconnect system 20 is a fiber channel. The device 25 may be an I/O subsystem, a Redundant Array of Inexpensive Disks (RAID) storage subsystem, a disk drive, a printer, a modem or a fax machine.

Figure 2 illustrates components within the device 25 which relate to addressing where the interconnect system 20 is a Fiber Channel. These components comprise a

serial shift register 30, an intelligence unit 32, n hardware registers 35, n ID comparator circuits 40 and a final combinational circuit 45. In one embodiment, the serial shift register 30 is a 48-bit serial shift register. In alternative embodiments, the shift register 30 is a 16-bit or 32-bit serial shift register. In one embodiment, the combinational circuit 45 is an OR-gate. In another embodiment, the combinational circuit 45 comprises multiple logic gates. The intelligence unit 32 on board the device 25 loads the IDs into the hardware registers 35. The hardware registers 35 hold n number of IDs associated with the device 25. For a Fiber Channel, n may be as high as 125.

A fiber serial bit stream is transmitted across the Fiber Channel 20 and enters the serial shift register 30. The serial shift register 30 holds the frame header of the bit stream. The frame header contains an address or ID for designating a device or devices. In one embodiment, the ID is 8 bits designated as AL_PA. The 8-bit AL_PA is fed into the n ID comparator circuits 40. The comparator circuits 40 compare the AL_PA against the ID values stored in the n hardware registers 35. The result of all the comparator circuits 40 is then checked by the final combinational circuit 45 to see if any of the IDs (ID0 through IDn) match the AL_PA. The final combinational circuit 45 outputs a signal, ID-Match, which indicates that the ID on the Fiber Channel 20 matches one of the device's IDs. If the ID matches, then the device 25 assumes that the incoming frame is addressed to the device 25. This method involves a significant amount of hardware (registers and logic circuits), especially if the number of assigned IDs is large.

Figure 3 illustrates one embodiment of the present invention. Similar to the device 35 illustrated in Figure 2, the fiber serial bit stream enters a serial shift register 30 which holds the frame header. Instead of using individual hardware registers 35 and comparators 40 to check for a match, the device 25 in Figure 3 comprises a random access memory (RAM) 50 and a multiplexer 60. As shown in Figure 3, the 8-bit AL_PA is fed into an address input of the RAM 50. Each address of the RAM 50 corresponds to an ID that the device 25 should or should not respond to. In one embodiment, the RAM 50 is configured as a 256 x 1 RAM because the incoming ID is 8 bits wide, and the RAM allows for 256 possible IDs. In another embodiment, the RAM 50 is configured as a 16 x 16 RAM. Those of ordinary skill in the art will appreciate that other RAM configurations may be used without departing from the scope of the invention.

The use and operation of the RAM 50 will now be described with reference to Figure 3. During initialization, an intelligence unit 55 accesses each location in the

RAM 50 via the DATA IN port and the ADDR (address) port shown in Figure 3. This intelligence unit 55 may be a microprocessor, a sequencer, or a controller. In a preferred embodiment, this intelligence unit 55 is on-board the device 25 such that each device 25 has its own intelligence unit 55. In another embodiment, the intelligence unit is a separate device (not shown) outside the device 25. The intelligence unit 55 writes a '0' in all locations (IDs) within the RAM 50 that the device 25 should not respond to and writes a '1' in all locations (IDs) that the device 25 should respond to.

After initialization, an AL_PA is fed into the ADDR (address) input port of the RAM 50. If the AL_PA is equal to an address that has been written with a '1' in the RAM's memory location (a location (ID) to which the device 25 is programmed to respond), a '1' will appear on the 1-bit data output, ID-Match, indicating a match. If the AL-PA is equal to an ID that has not been programmed with a '1,' then a '0' will appear on the 1-bit data output, ID-Match, indicating there is no match.

The present method and apparatus results in a significant reduction in hardware. For example, the use of the RAM 50 and the elimination of the comparators 40, 45 results in a smaller chip area, which lowers the manufacturing costs. The present method and apparatus also performs a compare operation in approximately the same amount of time as existing hardware logic circuits and registers. This is particularly advantageous for devices that can make use of multiple IDs.

While embodiments and applications of this invention have been shown and described, it will be apparent to those skilled in the art that various modifications are possible without departing from the scope of the invention. It is, therefore, to be understood that within the scope of the appended claims, this invention may be practiced otherwise than as specifically described.

WHAT IS CLAIMED IS:

1. An apparatus which compares a numeric address transmitted across a interconnect system with multiple addresses assigned to a device to determine if the transaction transmitted on the interconnect system is intended for this device, said apparatus comprising:

a random access memory with a plurality of memory locations which correspond to possible addresses to which the device could respond, said random access memory storing a '1' in each memory location corresponding to one of the device's assigned addresses and a storing a '0' for each memory location not corresponding to one of the device's assigned addresses, said random access memory further comprising:

an address input which receives an address from the interconnect system; and

a data output which informs the device whether the address received from the interconnect system matches one of the device's assigned addresses.

2. The apparatus of Claim 1, wherein the interconnect system is a Small Computer Standard Interface (SCSI) bus.

3. The apparatus of Claim 1, wherein the interconnect system is a Fiber Channel.

4. The apparatus of Claim 1, further comprising an intelligence unit, said intelligence unit writing a '1' in each memory location within the random access memory which corresponds to one of the device's assigned addresses, said intelligence unit writing a '0' in each memory location within the random access memory which does not correspond to one of the device's assigned addresses.

5. The apparatus of Claim 4 wherein the intelligence unit is a microprocessor.

6. The apparatus of Claim 4, wherein the intelligence unit is a microprocessor.

7. The apparatus of Claim 4, wherein the intelligence unit is a controller.

8. The apparatus of Claim 4, wherein the intelligence unit is a sequencer.

9. The apparatus of Claim 1, wherein the device is an I/O subsystem.

10. The apparatus of Claim 1, wherein the device is a disk drive.

11. The apparatus of Claim 1, wherein the device is a Redundant Array of Inexpensive Disks.

12. The apparatus of Claim 1, wherein the address transmitted across the interconnect system and the device's assigned addresses are each eight bits long, and wherein the random access memory has 256 memory locations corresponding to the 256 possible addresses assigned to the device.

13. The apparatus of Claim 3, further comprising a serial shift register which receives a fiber serial bit stream and transmits a part of the header containing an address to the random access memory.

14. A method of comparing a numeric address transmitted across a interconnect system with multiple addresses assigned to a device to determine if the transaction transmitted on the interconnect system is intended for this device, said method comprising:

receiving an address transmitted on the interconnect system into an address input of a random access memory, said random access memory storing a '1' in each memory location corresponding to one of the device's assigned addresses and storing a '0' for each memory location not corresponding to one of the device's assigned addresses;

outputting a '1' from a data output port of the random access memory if the address transmitted on the interconnect system is equal to any of the addresses assigned to the device; and

outputting a '0' from the data output port of the random access memory if the address transmitted on the interconnect system is not equal to an address assigned to the device.

15. The method of Claim 14, further comprising:

writing a '1' in each memory location within the random access memory which corresponds to one of the device's assigned addresses; and

writing a '0' in each memory location within the random access memory which does not correspond to one of the device's assigned addresses.

16. The method of Claim 14, wherein the interconnect system is a Small Computer Standard Interface (SCSI) bus.

17. The method of Claim 14, wherein the interconnect system is a Fiber Channel.

18. An apparatus which compares a numeric address transmitted across a interconnect system with a device's assigned addresses to determine if the impending transaction transmitted on the interconnect system is intended for the device, said apparatus comprising:

a random access memory with a plurality of memory locations which correspond to possible addresses to which the device could respond, said random access memory storing a '1' in each memory location corresponding to one of the device's assigned addresses and storing a '0' for each memory location not corresponding to one of the device's assigned addresses, said random access memory receiving an address from the interconnect system and outputting a data value to inform the device whether the address received from the bus matches one of the device's assigned addresses.

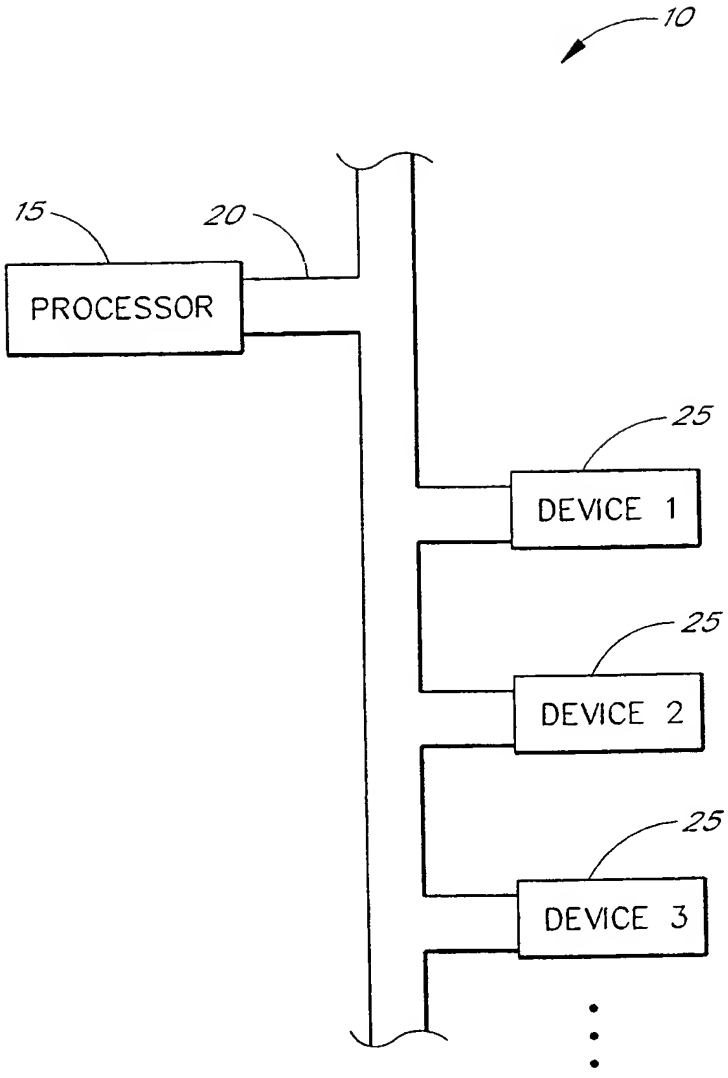

FIG. 1

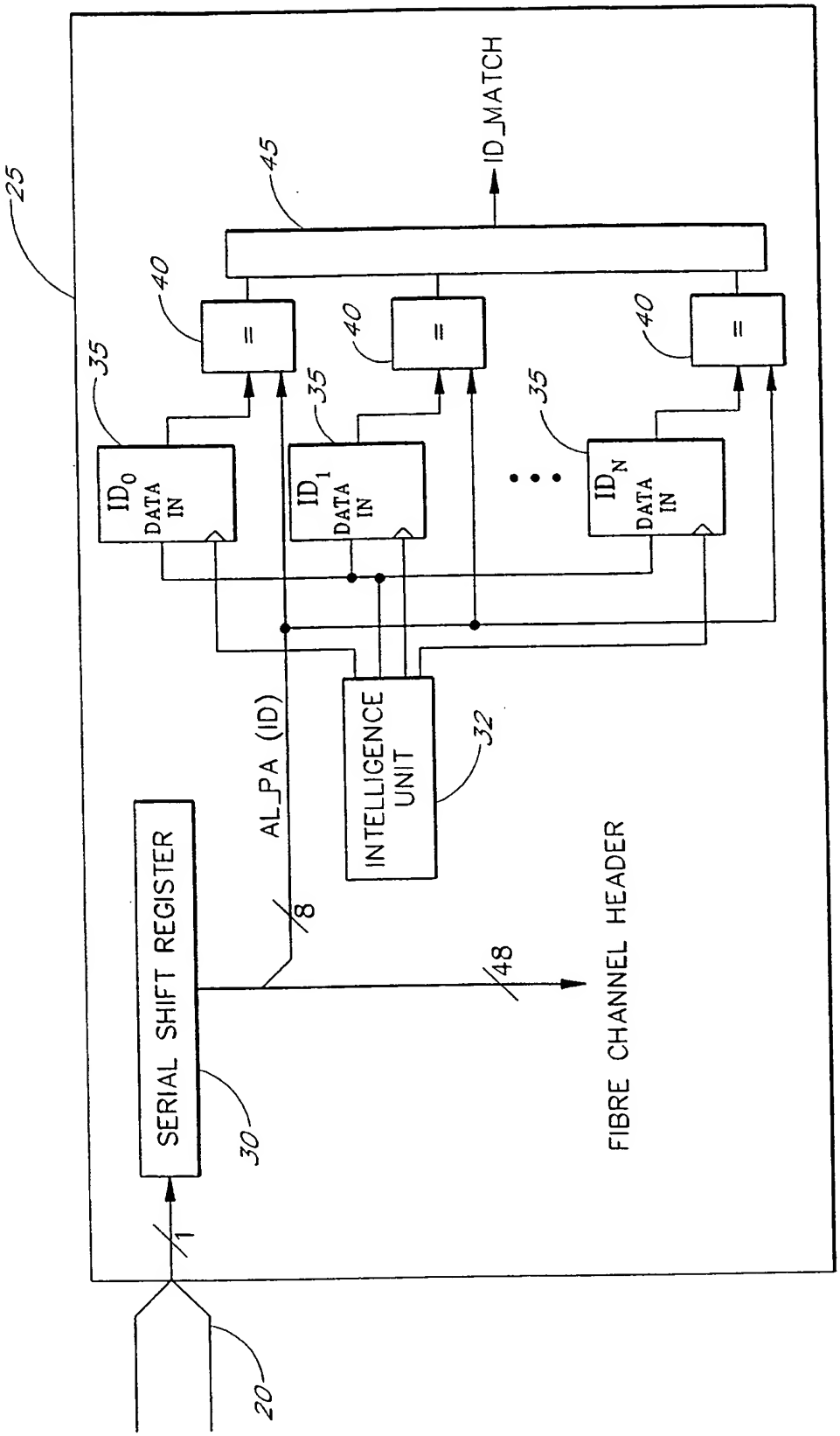
25
ID_MATCH
45
40
=
40
=
40
=
35
35
35
ID_0 DATA IN
ID_1 DATA IN
ID_N DATA IN
INTELLIGENCE UNIT
32
AL_PA (ID)
8
48
FIBRE CHANNEL HEADER
SERIAL SHIFT REGISTER
30
1
20

FIG. 2

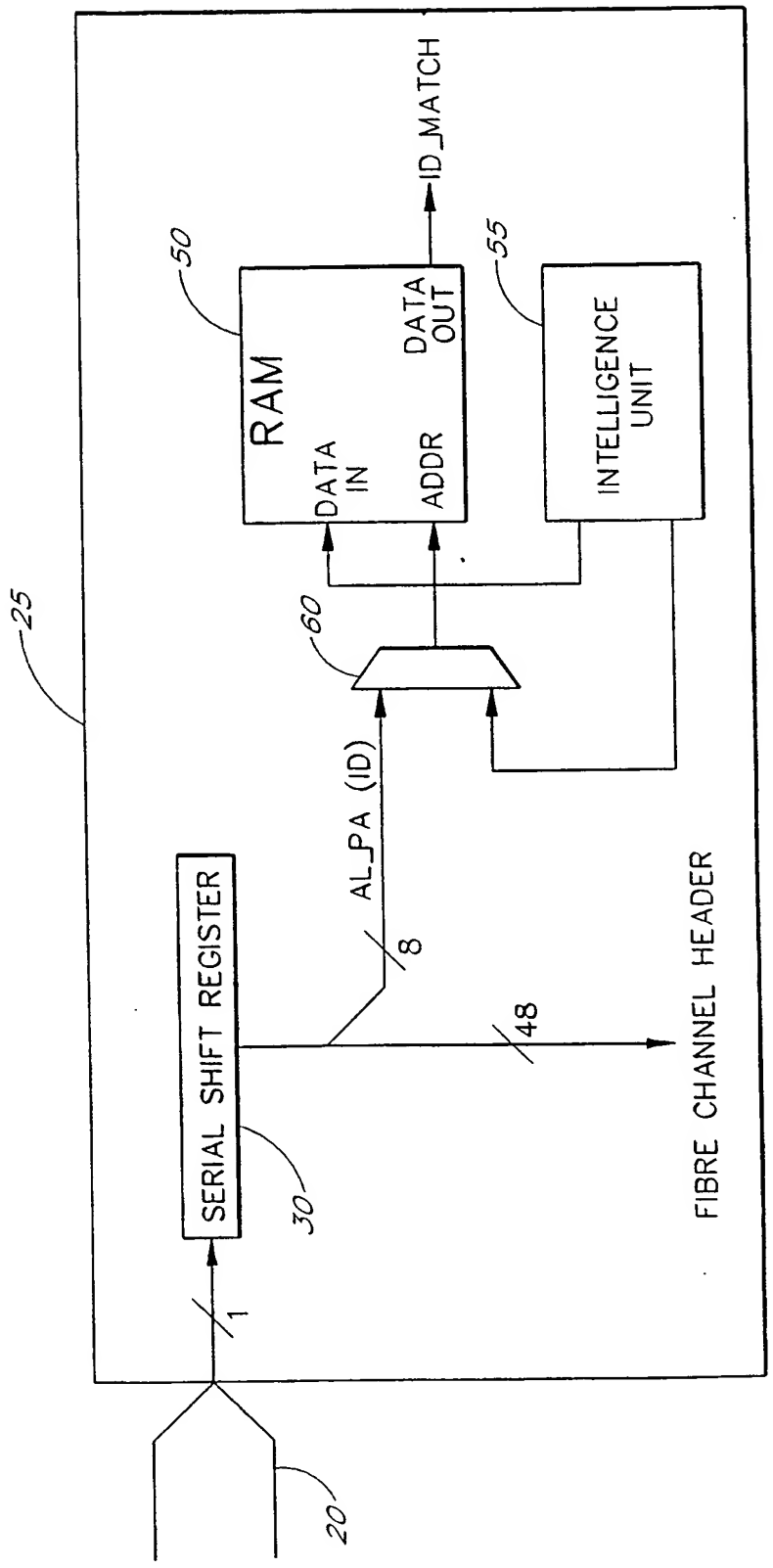
25
50
RAM
DATA IN
ADDR
DATA OUT
ID_MATCH
55
INTELLIGENCE UNIT
60
AL_PA (ID)
8
48
SERIAL SHIFT REGISTER
30
1
20
FIBRE CHANNEL HEADER

FIG. 3

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 99/20253

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F13/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 5 664 221 A (AMBERG MARK F. ET AL) 2 September 1997 (1997-09-02) column 1, line 21 - line 62 column 2, line 6 - line 50 column 3, line 18 -column 4, line 11 abstract; claims 1-3; figure 1 ---	1,2,4-6, 14-16,18 3,7-13, 17
A	US 5 204 669 A (DORFE STEVEN G ET AL) 20 April 1993 (1993-04-20) column 2, line 45 -column 4, line 6 column 5, line 4 - line 60 column 6, line 14 -column 7, line 54 column 9, line 22 -column 10, line 45 abstract; claims 1-3; figures 1,5 --- -/--	1-18

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 336 708 A (CONVERGENT TECHNOLOGIES INC) 11 October 1989 (1989-10-11) column 2, line 28 - line 62 column 3, line 27 -column 4, line 22 column 7, line 20 -column 8, line 14 abstract; claims 1-3; figures 1-3	1-18

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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